

**Amendments to the Claims**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

Claim 1 (currently amended) A memory pumping circuit comprising:

a DRAM cell used as a charging capacitor of the memory pumping circuit for enhancing the capacitance, wherein the DRAM cell comprising a MOS transistor and a storage capacitor;

a current source coupled to the DRAM cell for providing a charge current to the DRAM cell;

a node located between the current source and the DRAM cell for providing a pumping voltage used as a voltage source of a word line, and

a driving circuit for generating a clock signal to drive the DRAM cell;

wherein the MOS transistor has a source, a drain, and a gate connected together to the node and to one plate of the storage capacitor, and

wherein another plate of the storage capacitor is connected to receive the clock signal of the driving circuit.

Claim 2-6 (canceled)

Claim 7 (previously presented) The memory pumping circuit according to Claim 1, wherein said driving circuit is an inverter.

Claim 8 (currently amended) The memory pumping circuit according to Claim [[6]] 1, wherein the driving circuit comprises a PMOS transistor and a NMOS transistor, and generates the clock signal according to a first clock signal and a second clock signal.

Claim 9 (currently amended) A memory pumping circuit comprises:

a current source for providing a charge current;

a DRAM cell as a charging capacitor of the pumping circuit, the DRAM cell having an output port for providing a pumping voltage

used as a voltage source of a word line, the output port coupled to the current source for receiving the charge current, wherein the DRAM cell comprising a MOS transistor and a storage capacitor; and

a driving circuit for generating a first clock signal to the DRAM cell for driving the DRAM cell;

wherein the MOS transistor has a source, a drain, and a gate connected together to the output port of the DRAM cell and to one plate of the storage capacitor, and

wherein another plate of the storage capacitor is connected to receive the first clock signal of the driving circuit.

Claim 10-11 (canceled)

Claim 12 (previously presented) The memory pumping circuit according to Claim 9 wherein the driving circuit is an inverter.

Claim 13 (previously presented) The memory pumping circuit according to Claim 9 wherein the driving circuit comprises a PMOS transistor and a NMOS transistor, and generates the first clock signal according to a second clock signal and a third clock signal.